

CLAIMS

What is claimed is:

1. 1. A method of debugging an executing service on a pipelined CPU architecture, the method comprising:
 - 2 setting a breakpoint within an executing service;
 - 3 saving a minimum state of the executing service;
 - 4 altering a program counter of the executing service;
 - 5 restoring the program counter of the executing service; and
 - 6 restoring the state of the executing service.
1. 2. The method of claim 1 further comprising:executing debug commands within the executing service.
1. 3. The method of claim 1 wherein setting the breakpoint further comprises:
 - 2 locating an original instruction within the executing service to set the breakpoint;
 - 3 inserting a breakpoint instruction at the breakpoint;
 - 4 starting the executing service;
 - 5 waiting for the breakpoint to execute;
 - 6 waiting for memory fetches and configuration loads to complete; and
 - 7 restoring the original instruction at the breakpoint location.
1. 4. The method of claim 1 wherein setting the breakpoint comprises:
 - 2 altering an instruction within the executing service at a breakpoint location; and
 - 3 invalidating a page cache of the executing service.

1 5. The method of claim 1 wherein setting the breakpoint comprises:

2 setting a breakpoint register to point to a breakpoint location.

1 6. The method of claim 1 wherein saving a minimum state comprises:

2 saving the executing service registers; and

3 flushing a pipeline of the executing service.

1 7. The method of claim 6 wherein flushing the pipeline further comprises:

2 determining if registers are unstable;

3 if registers are unstable, saving the value of any registers that change after each
4 pipeline cycle; and

5 if the breakpoint location is set on a location that uses old values of registers,
6 saving the old values of the registers before new values are written to the
7 registers.

8. The method of claim 7 wherein registers are scalar registers or predicate registers.

1 9. The method of claim 1 wherein altering the program counter further comprises:

2 setting the program counter of the executing service to point to a save stub;

3 starting execution of the executing service;

4 executing the breakpoint;

5 storing configuration registers of the executing service;

6 saving values of scalar and predicate registers;

7 saving pipeline registers; and

8 storing a stack pointer value for a breakpoint location.

1 10. The method of claim 1 wherein restoring the program counter further comprises:

2 setting the program counter of the executing service to point to a restore stub;

3 and

4 starting the executing service at the breakpoint.

1 11. The method of claim 1 wherein restoring the state further comprises:

2 if a breakpoint location is on an instruction that does not make use of old values,

3 restoring stable registers;

4 if the breakpoint location is on an instruction that does make use of old values,

5 restoring unstable registers, and

6 reloading the pipeline;

7 altering the program counter of the executing service to point to the breakpoint

8 location; and

9 starting execution of the executing service at the breakpoint location.

12. The method of claim 1 further comprising:

2 fetching a page of memory of the executing service into an instruction cache;

3 checking for a checksum error within the page of memory; and

4 if the executing service is set to reject the checksum error,

5 saving the page of memory,

6 inserting a breakpoint into the saved page of memory,

7 altering an instruction pointer to the saved page of memory, and

8 processing the saved page of memory.

1 13. A method of debugging an executing service on a pipelined CPU architecture, the
2 method comprising:

3 setting a breakpoint at a last safe point;

4 saving a minimum state of the executing service;

5 simulating instructions of the executing service from the last safe point to the

6 breakpoint;

7 executing debug commands within the executing service; and

8 restoring the state of the executing service.

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1 14. The method of claim 13 wherein restoring further comprises:

2 storing the simulated state of the executing server to the CPU; and restoring

3 an original execution.

1 15. The method of claim 13 wherein simulating further comprises single stepping

2 through a set of unsafe instructions, the set of unsafe instructions are between the

3 last safe point and a next safe point.

1 16. A method of debugging an executing service on a pipelined CPU architecture

2 without hardware interlocks, the method comprising:

3 fetching a page of memory of the executing service into an instruction cache;

4 checking for a checksum error within the page of memory; and

5 if the executing service is set to reject the checksum error,

6 saving the page of memory,

7 inserting a breakpoint into the saved page of memory,

8 altering an instruction pointer to the saved page of memory, and

~~9~~ processing the saved page of memory.

17. The method of claim 16 wherein processing further comprises:

setting a breakpoint within an executing service;

saving a minimum state of the executing service;

altering a program counter of the executing service;

executing debug commands within the executing service

restoring the program counter of the executing service; and

restoring the state of the executing service.

1 18. A system for debugging an executing service on a pipelined CPU architecture
2 without hardware interlocks, the system comprising:
3 a debugger to set a breakpoint within an executing service and execute debug
4 commands within the executing service;
5 a save stub to save a minimum state of the executing service and alter a program
6 counter of the executing service;
7 a processing engine to execute the breakpoint; and
8 a restore stub to restore the state of the executing service.

1 19. The system of claim 18 wherein the debugger is further operable to locate an
2 original instruction within the executing service to set the breakpoint, insert a
3 breakpoint instruction at the breakpoint, start the executing service, wait for the
4 breakpoint to execute, wait for memory fetches and configuration loads to complete,
5 and restore the original instruction at the breakpoint location.

1 20. The system of claim 18 wherein the debugger is further operable to alter an
2 instruction within the executing service at a breakpoint location, and invalidate a
3 page cache of the executing service.

1 21. The system of claim 18 wherein the debugger is further operable to set a breakpoint
2 register to point to a breakpoint location.

1 22. The system of claim 18 wherein the save stub is further operable to save the
2 executing service registers.

1 23. The system of claim 18 wherein the processing engine is further operable to flush a
2 pipeline of a set of pipeline instructions of the executing service.

1 24. The system of claim 22 wherein the debugger is further operable to determine if
2 registers are unstable, save the value of any registers that change after each pipeline
3 cycle if registers are unstable, save the old values of the registers before new values
4 are written to the registers, and if the breakpoint location is set on a location that
5 uses old values of registers.

1 25. The method of claim 24 wherein registers are scalar registers or predicate registers.

1 26. The system of claim 18 wherein the debugger is further operable to set the program
2 counter of the executing service to point to a save stub, start execution of the
3 executing service, execute the breakpoint, store configuration registers of the
4 executing service, save values of the scalar and predicate registers, and save pipeline
5 registers.

1 27. The system of claim 18 wherein the debugger is further operable to set the program
2 counter of the executing service to point to a restore stub, and start the executing
3 service at the breakpoint.

1 28. The system of claim 18 wherein the restore stub is further operable to:

2 if a breakpoint location is on an instruction that does not make use of old values,

3 restore stable registers;

4 if the breakpoint location is on an instruction that does make use of old values,

5 restore unstable registers, and

6 reload the pipeline;

7 alter the program counter of the executing service to point to the breakpoint

8 location; and

9 start execution of the executing service at the breakpoint location.

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11 29. The system of claim 28 wherein the restore stub is further operable to reload the

12 pipeline state directly.

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14 30. The system of claim 28 wherein the restore stub is further operable to re-execute

15 the original instructions within the pipeline to recreate the pipeline at a time of the

16 breakpoint.

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18 31. The system of claim 18 wherein the processing engine is further operable to:

19 fetch a page of memory of the executing service into an instruction cache; and

20 check for a checksum error within the page of memory.

1 32. The system of claim 18 wherein the debugger is further operable to:

2 if the executing service is set to reject the checksum error,

3 save the page of memory,

4 insert a breakpoint into the saved page of memory,

5 alter an instruction pointer to the saved page of memory, and

6 process the saved page of memory.

1 33. A system for debugging an executing service on a pipelined CPU architecture, the
2 system comprising:

3 a save stub to save a minimum state of the executing service;

4 a restore stub to restore the state of the executing service; and

5 a debugger to set a breakpoint at a last safe point, simulate instructions of the

6 executing service from the last safe point to the breakpoint, and execute

7 debug commands within the executing service.

1 34. The system of claim 33 wherein the restore stub further stores the simulated state
2 of the executing service to the CPU, and resumes an original execution.

1 35. The system of claim 33 wherein the debugger is further operable to single step
2 through a set of unsafe instructions, the set of unsafe instructions are between the
3 last safe point and a next safe point.

1 36. A system for debugging an executing service on a pipelined CPU architecture, the
2 system comprising:

3 a processing engine to fetch a page of memory of the executing service into an
4 instruction cache, and check for a checksum error within the page of memory;

5 and

6 if the executing service is set to reject the checksum error, a debugger operable to
7 save the page of memory, insert a breakpoint into the saved page of memory,
8 alter an instruction pointer to the saved page of memory, and process the
9 saved page of memory.

1 37. The system of claim 36 wherein the debugger is further operable to set a
2 breakpoint within an executing service, save a minimum state of the executing
3 service, alter a program counter of the executing service, and execute debug
4 commands within the executing service.

1 38. The system of claim 37 further comprising:

2 a restore stub operable to restore the program counter of the executing service,
3 and restore the state of the executing service.

1 39. A system for debugging an executing service on a pipelined CPU architecture, the
2 system comprising:

3 means for setting a breakpoint within an executing service;
4 means for saving a minimum state of the executing service;
5 means for altering a program counter of the executing service;
6 means for restoring the program counter of the executing service; and
7 means for restoring the state of the executing service.

1 40. A system for debugging an executing service on a pipelined CPU architecture, the
2 system comprising:

3 means for setting a breakpoint at a last safe point;
4 means for saving a minimum state of the executing service;
5 means for simulating instructions of the executing service from the last safe point
6 to the breakpoint;
7 means for executing debug commands within the executing service; and
8 means for restoring the state of the executing service.

1 41. A system for debugging an executing service on a pipelined CPU architecture, the
2 system comprising:

3 means for fetching a page of memory of the executing service into an instruction
4 cache;

5 means for checking for a checksum error within the page of memory; and

6 if the executing service is set to reject the checksum error,

7 means for saving the page of memory,

8 means for inserting a breakpoint into the saved page of memory,

9 means for altering an instruction pointer to the saved page of memory,

10 and

11 means for processing the saved page of memory.

1 42. A computer readable medium comprising instructions, which when executed on a
2 processor, perform a method for debugging an executing service on a pipelined
3 CPU architecture, comprising:

4 setting a breakpoint within an executing service;

5 saving a minimum state of the executing service;

6 altering a program counter of the executing service;

7 restoring the program counter of the executing service; and

8 restoring the state of the executing service.

1 43. A computer readable medium comprising instructions, which when executed on a
2 processor, perform a method for debugging an executing service on a pipelined
3 CPU architecture, comprising:
4 setting a breakpoint at a last safe point;
5 saving a minimum state of the executing service;
6 simulating instructions of the executing service from the last safe point to the
7 breakpoint;
8 executing debug commands within the executing service; and
9 restoring the state of the executing service.

10 44. A computer readable medium comprising instructions, which when executed on a
11 processor, perform a method for debugging an executing service on a pipelined
12 CPU architecture, comprising:
13 fetching a page of memory of the executing service into an instruction cache;
14 checking for a checksum error within the page of memory; and
15 if the executing service is set to reject the checksum error,
16 saving the page of memory,
17 inserting a breakpoint into the saved page of memory,
18 altering an instruction pointer to the saved page of memory, and
19 processing the saved page of memory.